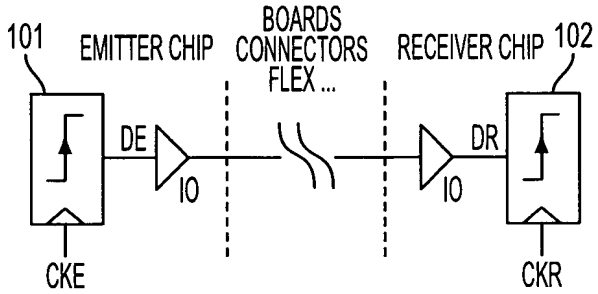

FIG. 1

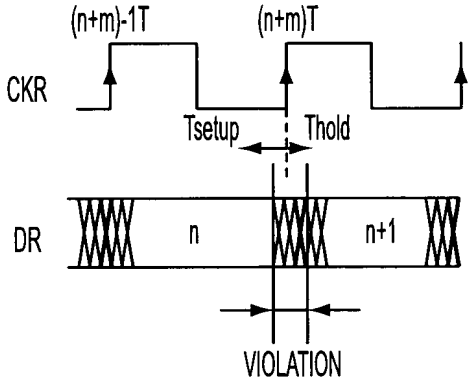

FIG. 2

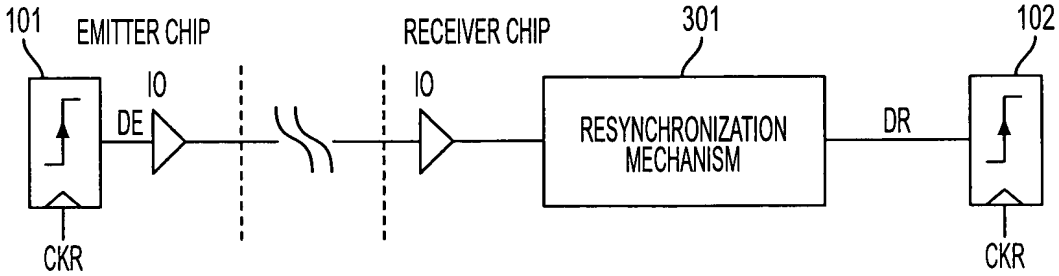

FIG. 3

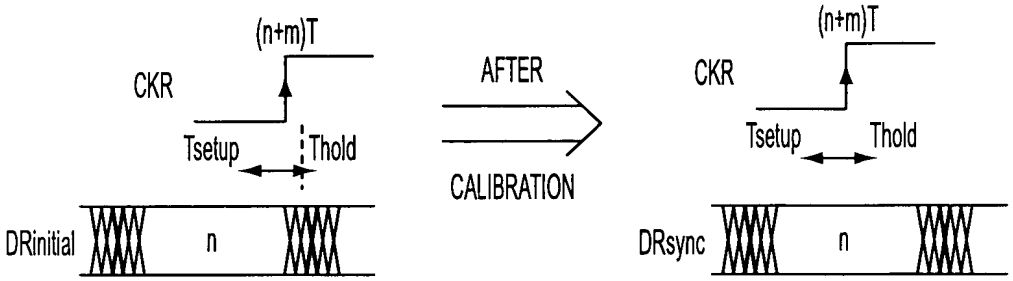
(n+m)T
CKR
Tsetup
Thold
DRinitial
n
AFTER
CALIBRATION
(n+m)T
CKR
Tsetup
Thold
DRsync
n

FIG. 4

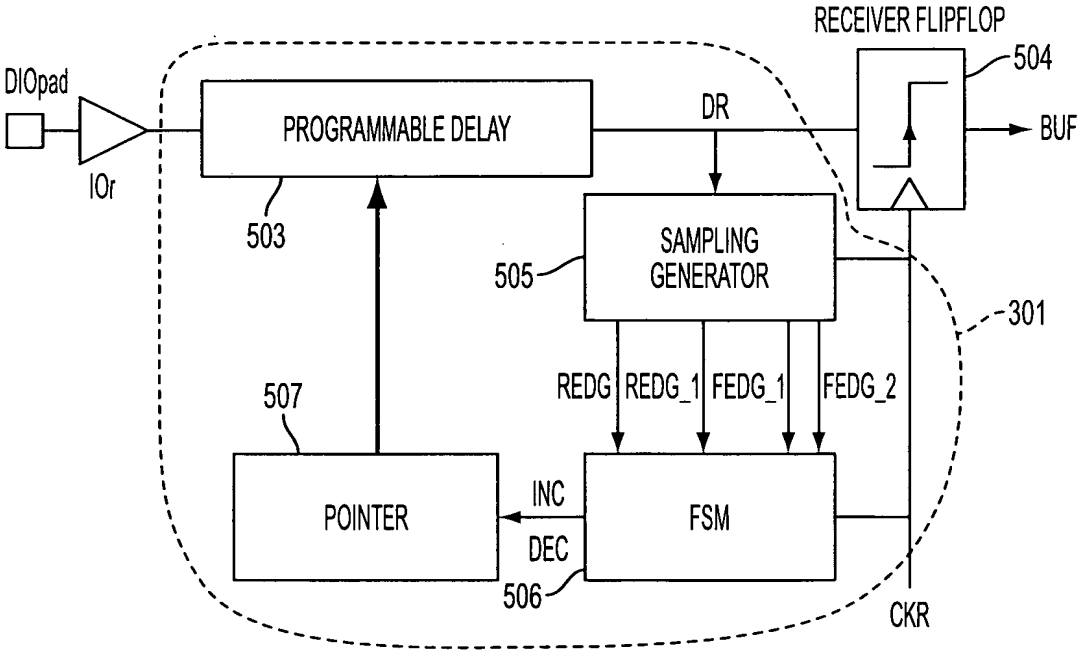
RECEIVER FLIPFLOP
504
DIOpad
IOr
PROGRAMMABLE DELAY
DR
BUF
503
SAMPLING GENERATOR
505
301
REDG
REDG_1
FEDG_1
FEDG_2
507
POINTER
INC
DEC
FSM
506
CKR

FIG. 5

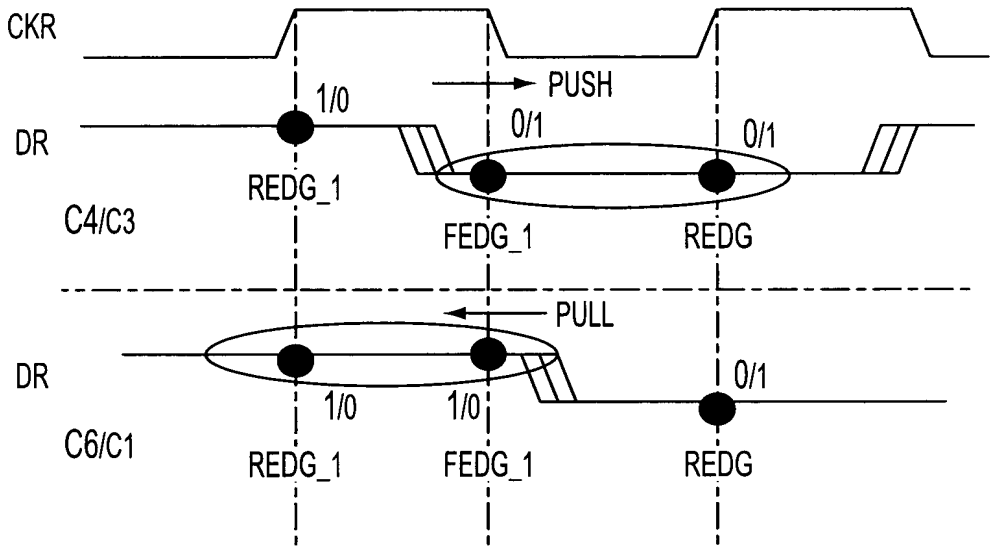
CKR
DR
C4/C3
1/0
REDG_1
PUSH
0/1
FEDG_1
0/1
REDG
PULL
DR
C6/C1
1/0
REDG_1
1/0
FEDG_1
0/1
REDG

FIG. 6

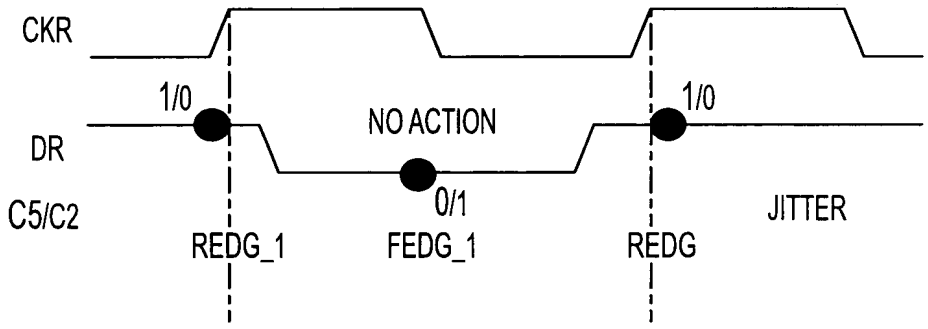
CKR
DR
C5/C2
1/0
REDG_1
NO ACTION
0/1
FEDG_1
1/0
REDG
JITTER

FIG. 7

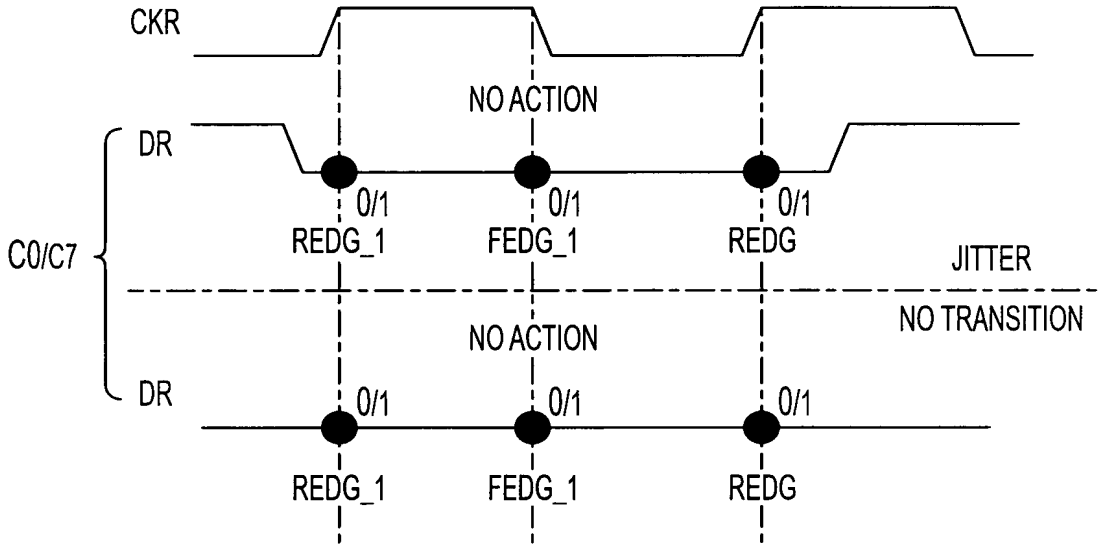
CKR
NO ACTION
DR
C0/C7
0/1
REDG_1
0/1
FEDG_1
0/1
REDG
JITTER
NO TRANSITION
NO ACTION
DR
0/1
REDG_1
0/1
FEDG_1
0/1
REDG

FIG. 8

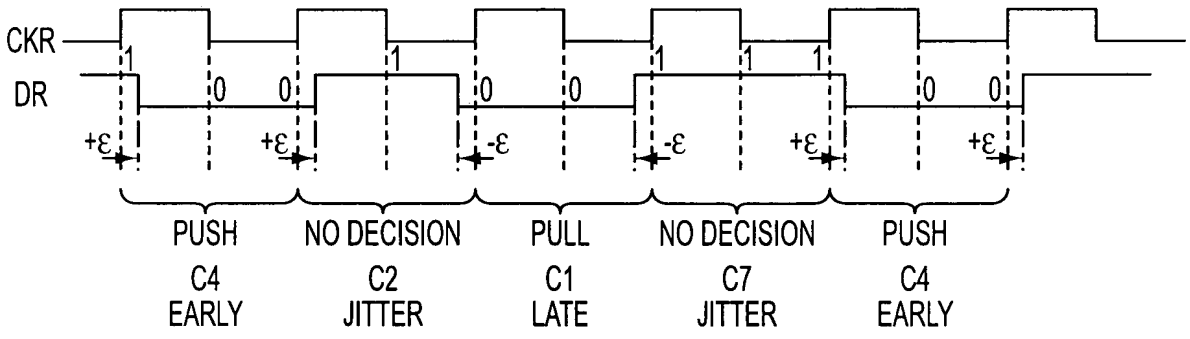
CKR
DR
1
0
0
1
0
0
1
1
1
0
0
+ε
+ε
-ε
-ε
+ε
+ε
PUSH
C4
EARLY
NO DECISION
C2
JITTER
PULL
C1
LATE
NO DECISION
C7
JITTER
PUSH
C4
EARLY

FIG. 9

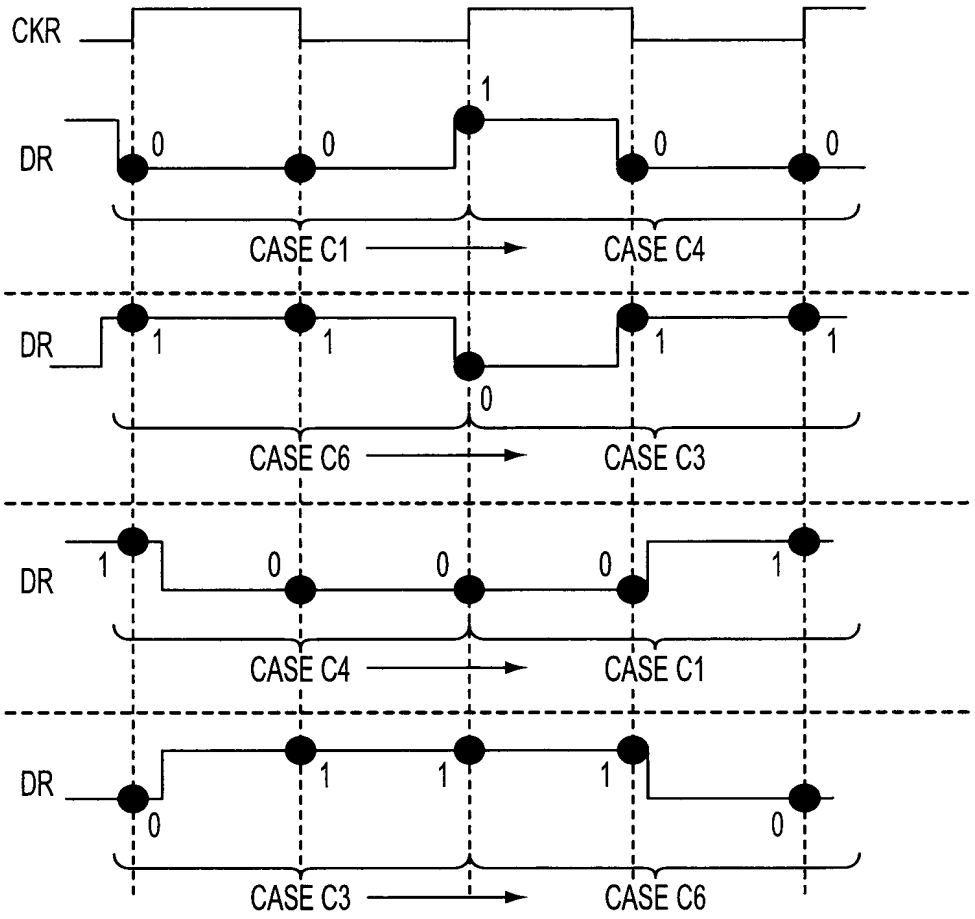
CKR
DR
0
0
1
0
0
CASE C1
CASE C4
DR
1
1
0
1
1
CASE C6
CASE C3
DR
1
0
0
0
1
CASE C4
CASE C1
DR
0
1
1
1
0
CASE C3
CASE C6

FIG. 10

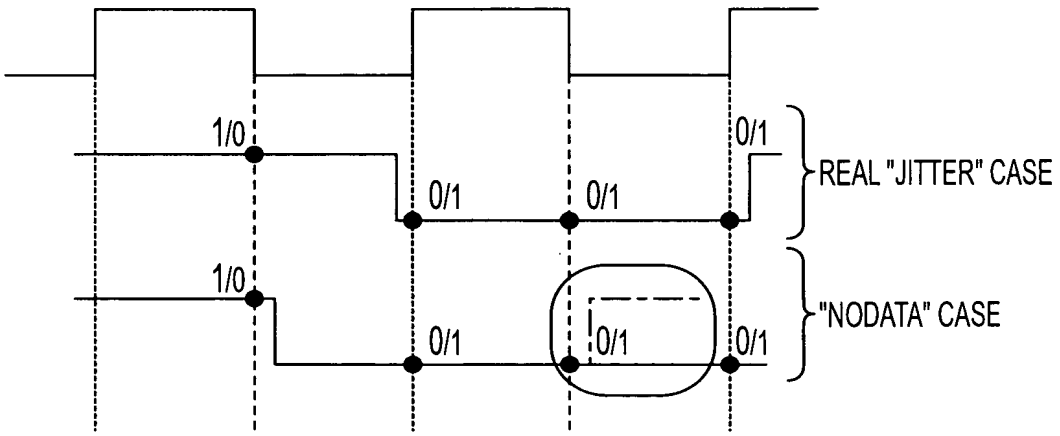
1/0
0/1
0/1
0/1
REAL "JITTER" CASE
1/0
0/1
0/1
0/1
"NODATA" CASE

FIG. 11

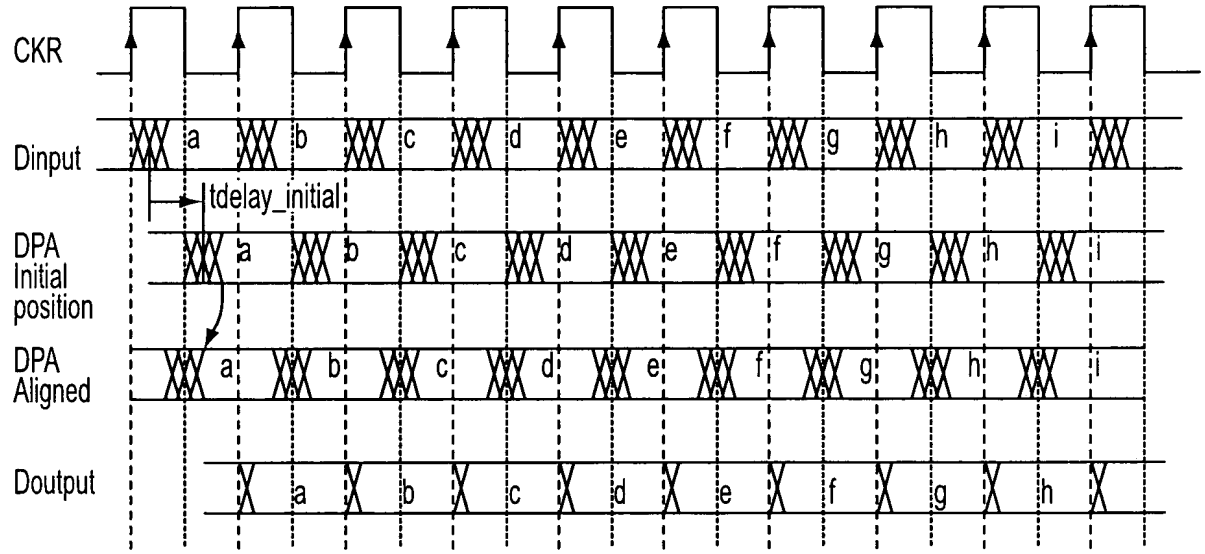
CKR
Dinput
tdelay_initial
DPA Initial position
DPA Aligned
Doutput

FIG. 12

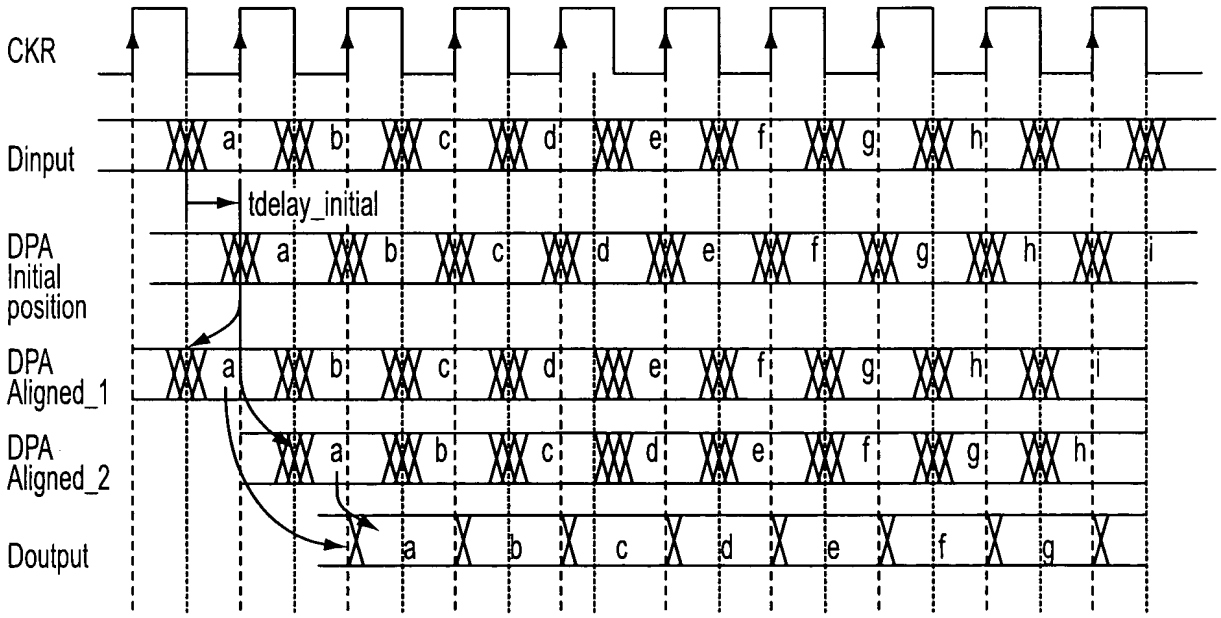
CKR
Dinput
tdelay_initial
DPA Initial position
DPA Aligned_1
DPA Aligned_2
Doutput

FIG. 13

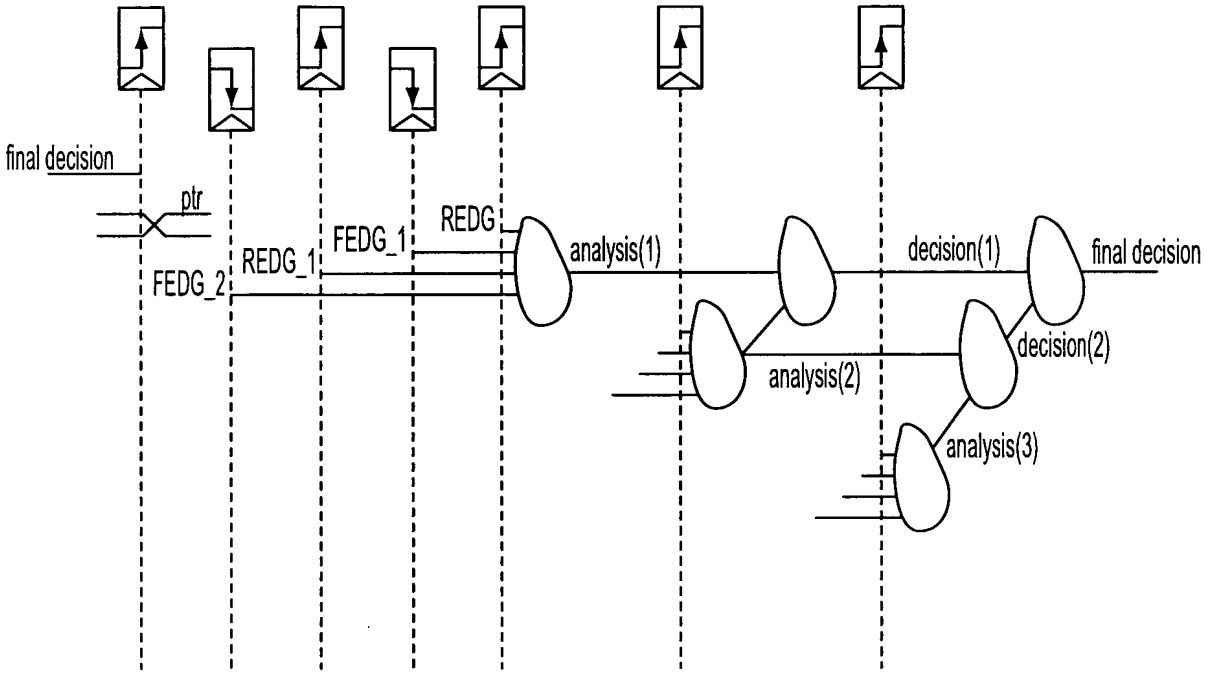
final decision
ptr
FEDG_2
REDG_1
FEDG_1
REDG
analysis(1)
decision(1)
final decision
analysis(2)
decision(2)
analysis(3)

FIG. 14

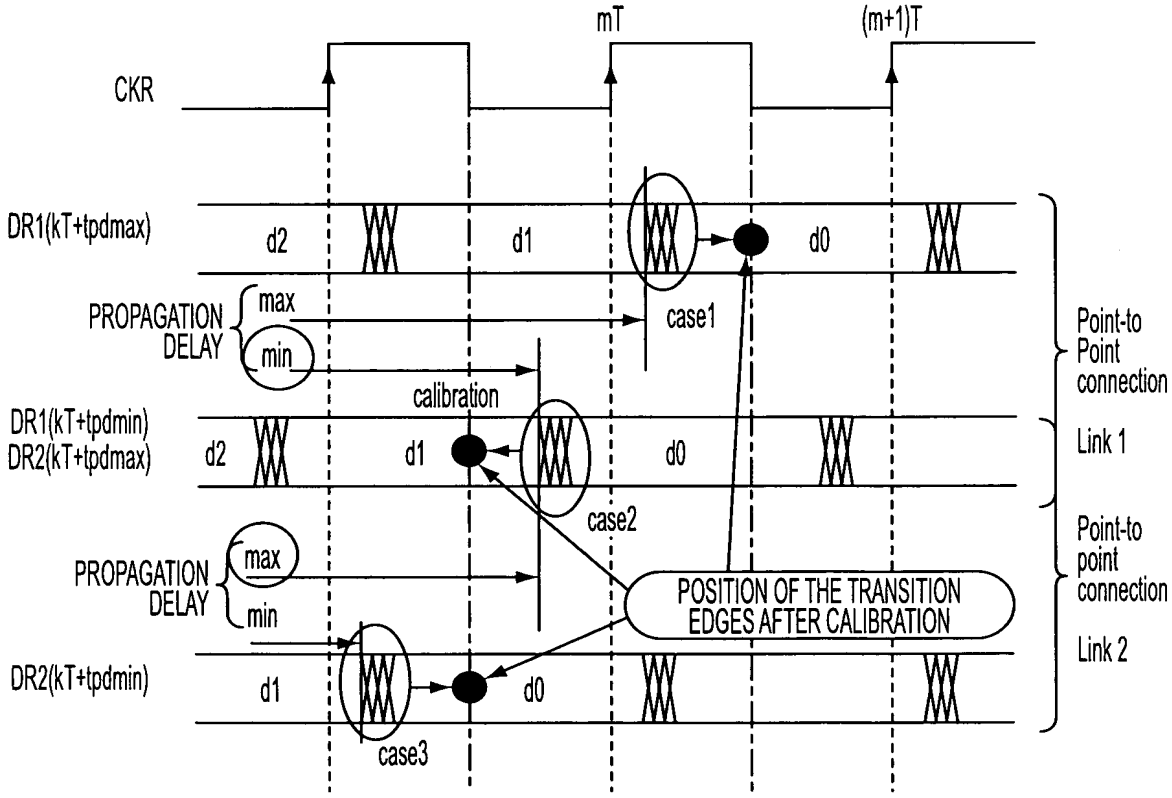
mT
(m+1)T
CKR
DR1(kT+tpdmax)
d2
d1
d0
PROPAGATION DELAY
max
min
case1
calibration
DR1(kT+tpdmin)
DR2(kT+tpdmax)
d2
d1
d0
case2
PROPAGATION DELAY
max
min
POSITION OF THE TRANSITION EDGES AFTER CALIBRATION
DR2(kT+tpdmin)
d1
d0
case3
Point-to Point connection
Link 1
Point-to point connection
Link 2

FIG. 15

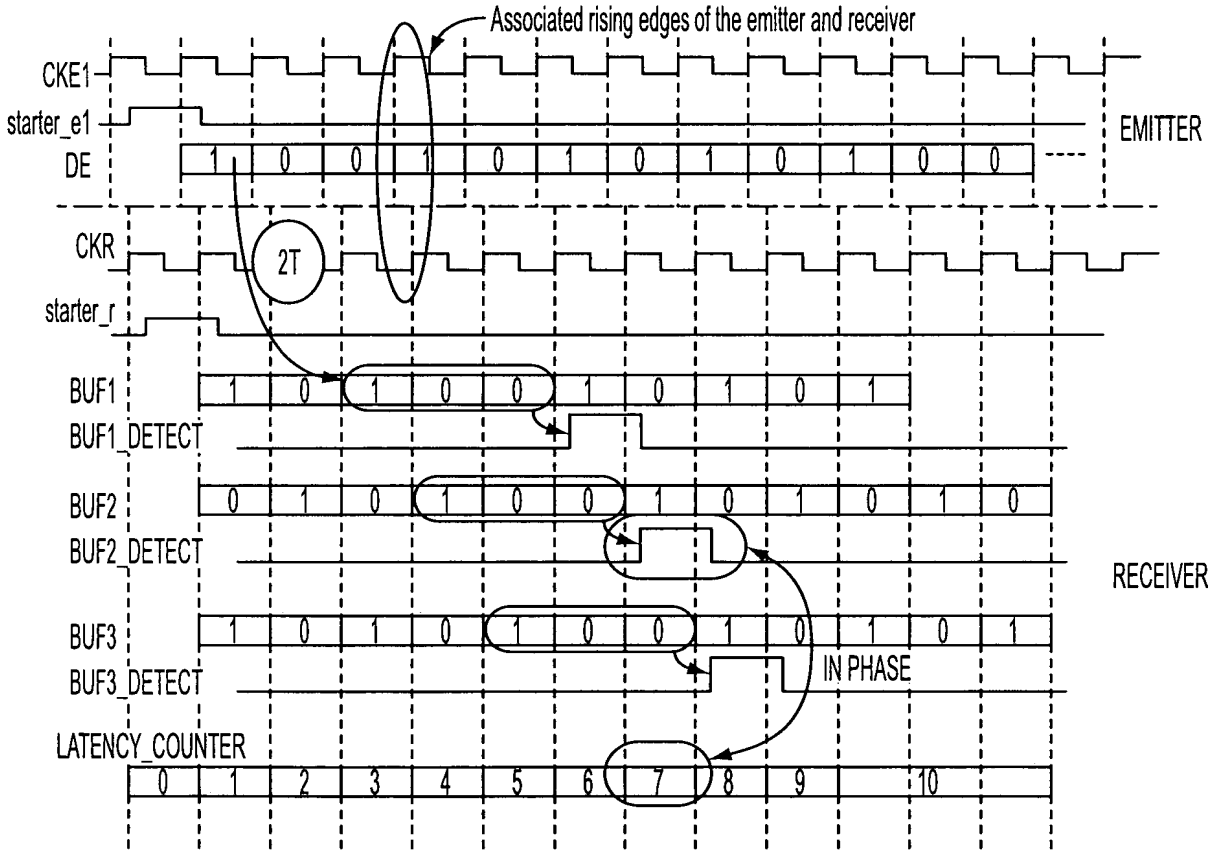
Associated rising edges of the emitter and receiver
CKE1
starter_e1
DE
EMITTER
CKR
2T
starter_r
BUF1
BUF1_DETECT
BUF2
BUF2_DETECT
RECEIVER
BUF3
BUF3_DETECT
IN PHASE
LATENCY_COUNTER
0 1 2 3 4 5 6 7 8 9 10

FIG. 16

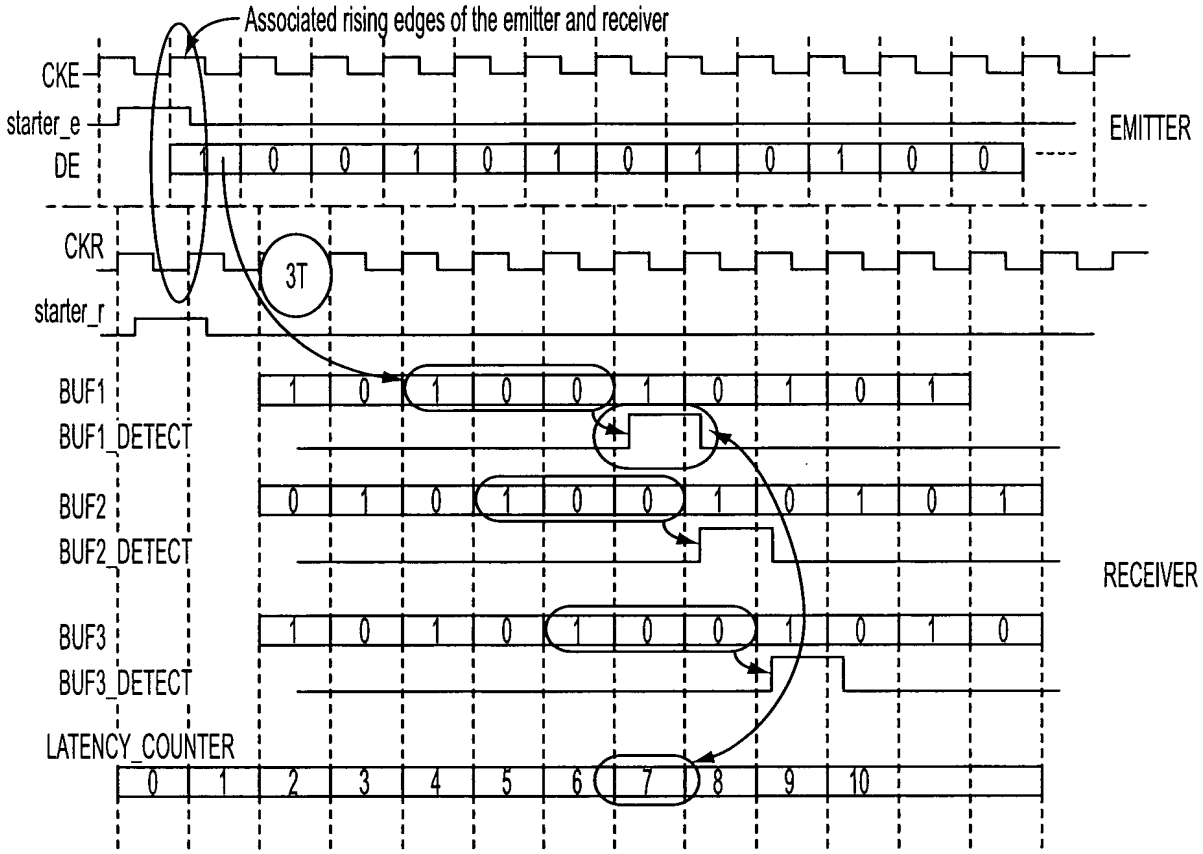
Associated rising edges of the emitter and receiver
CKE
starter_e
DE
EMITTER
CKR
3T
starter_r
BUF1
BUF1_DETECT
BUF2
BUF2_DETECT
BUF3
BUF3_DETECT
RECEIVER
LATENCY_COUNTER
0 1 2 3 4 5 6 7 8 9 10

FIG. 17

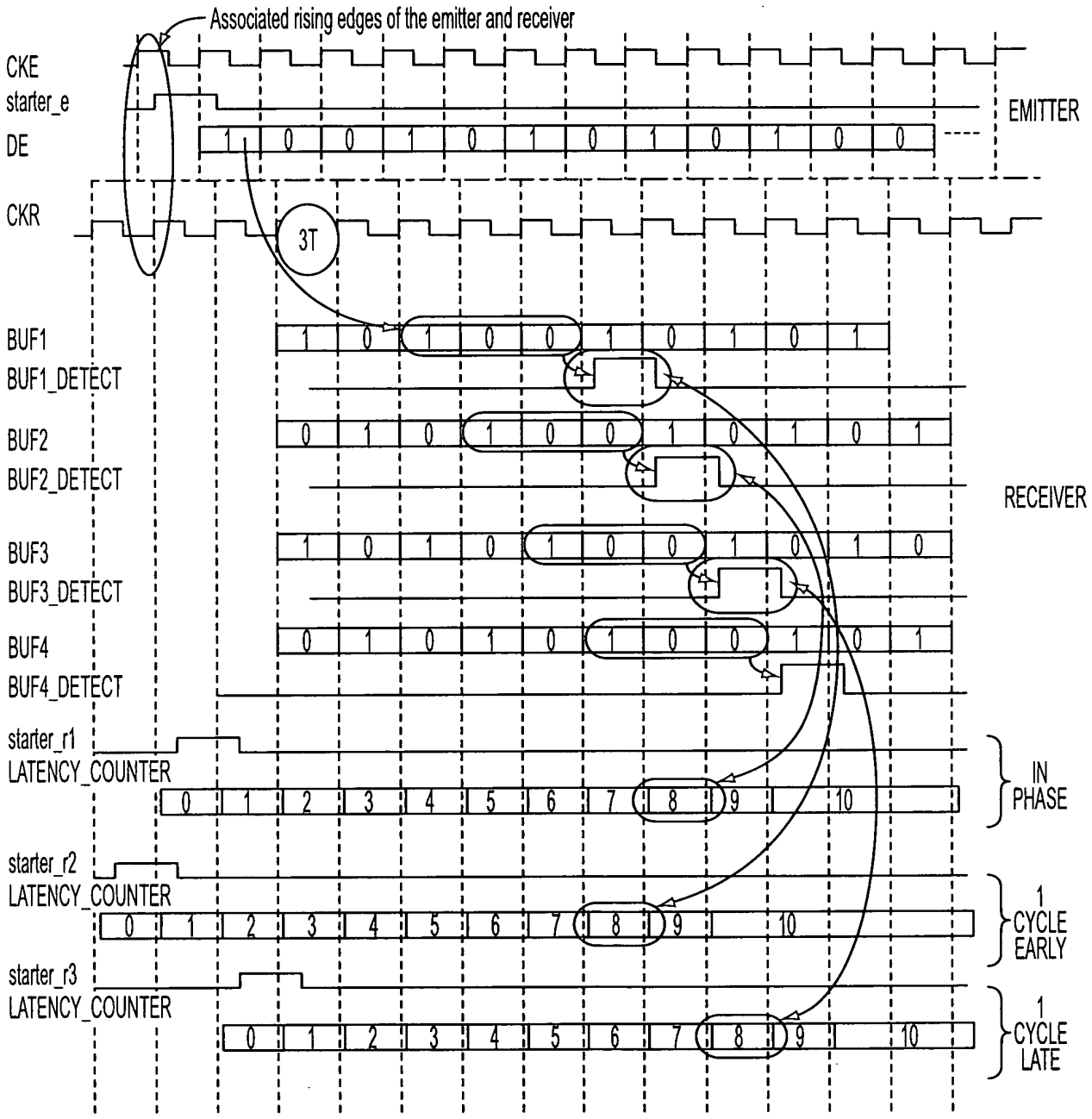
Associated rising edges of the emitter and receiver
CKE
starter_e
DE
EMITTER
CKR
3T
BUF1
BUF1_DETECT
BUF2
BUF2_DETECT
RECEIVER
BUF3
BUF3_DETECT
BUF4
BUF4_DETECT
starter_r1
LATENCY_COUNTER
IN PHASE
starter_r2
LATENCY_COUNTER
1 CYCLE EARLY
starter_r3
LATENCY_COUNTER
1 CYCLE LATE

FIG. 18

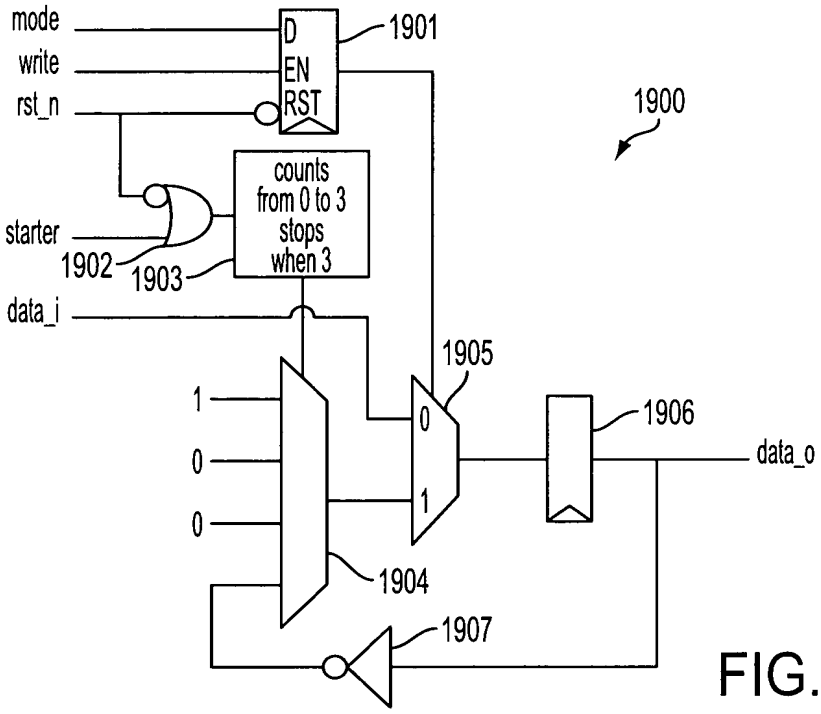
mode
write
rst_n
D
EN
RST
1901
1900
counts from 0 to 3 stops when 3
starter
1902
1903
data_i
1905
1
0
0
0
1
1906
data_o
1904
1907

FIG. 19

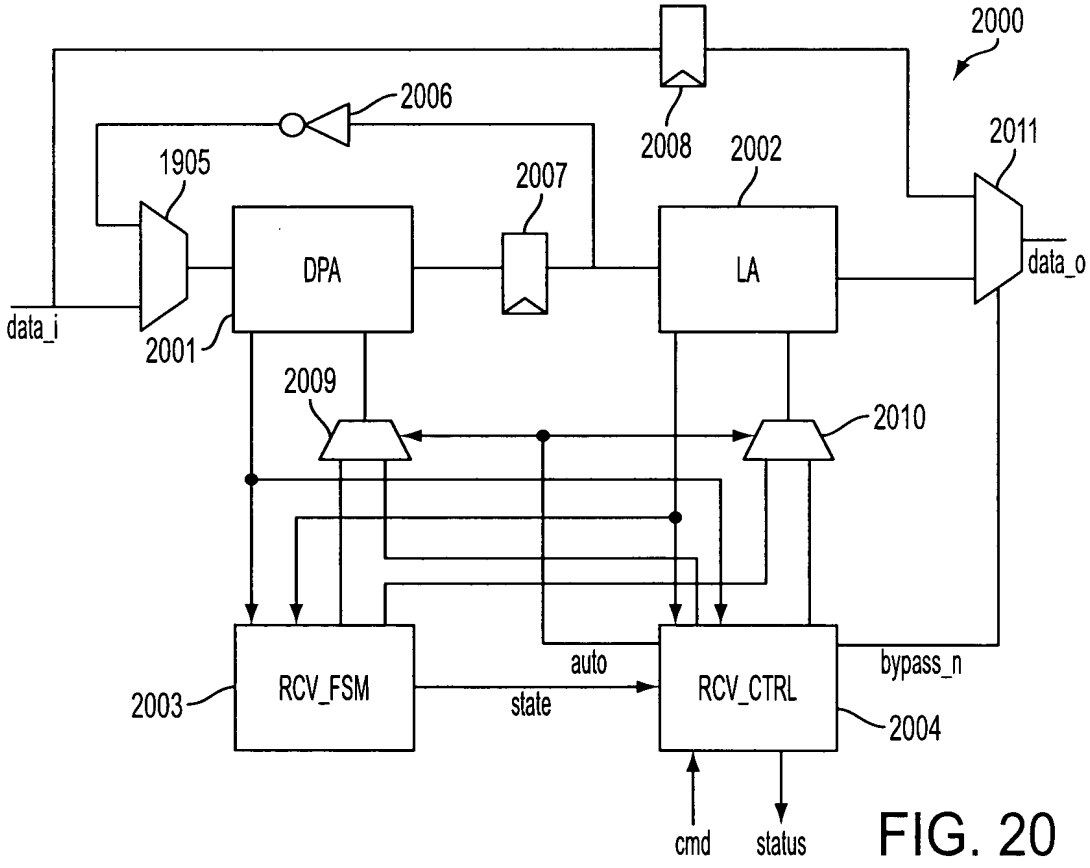
2000
2006
2008
2002
2011
1905
2007
DPA
LA
data_o
data_i
2001
2009
2010
RCV_FSM
auto
state
RCV_CTRL
bypass_n
2003
2004
cmd
status

FIG. 20

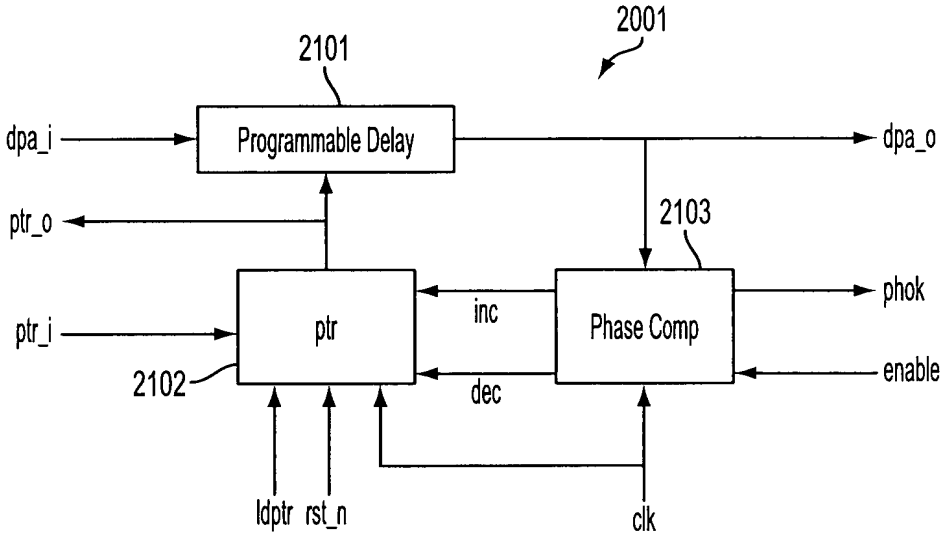

FIG. 21

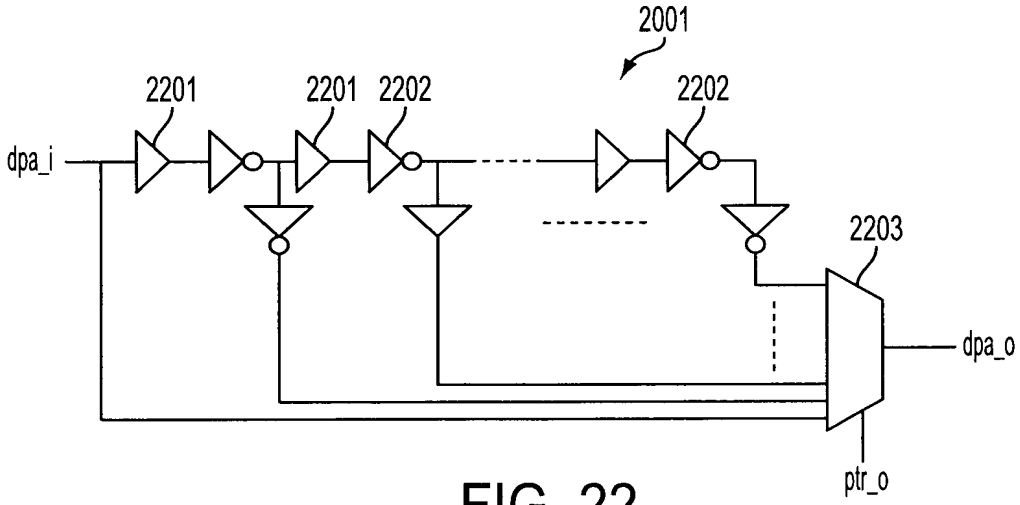

FIG. 22

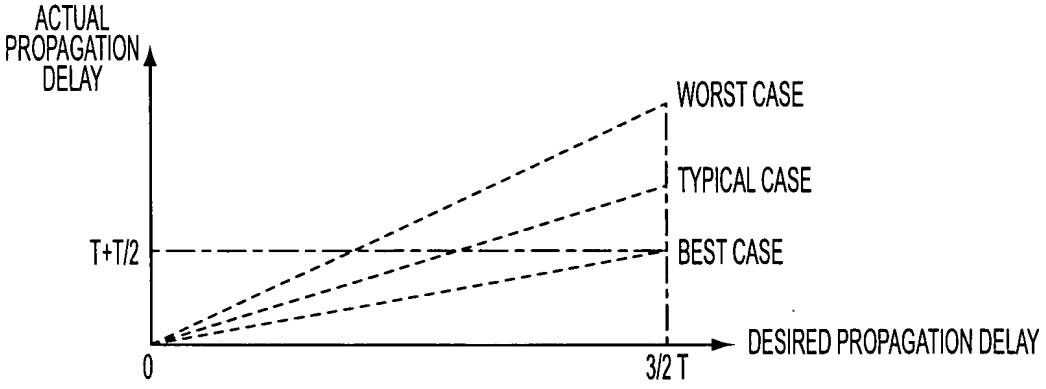

FIG. 23

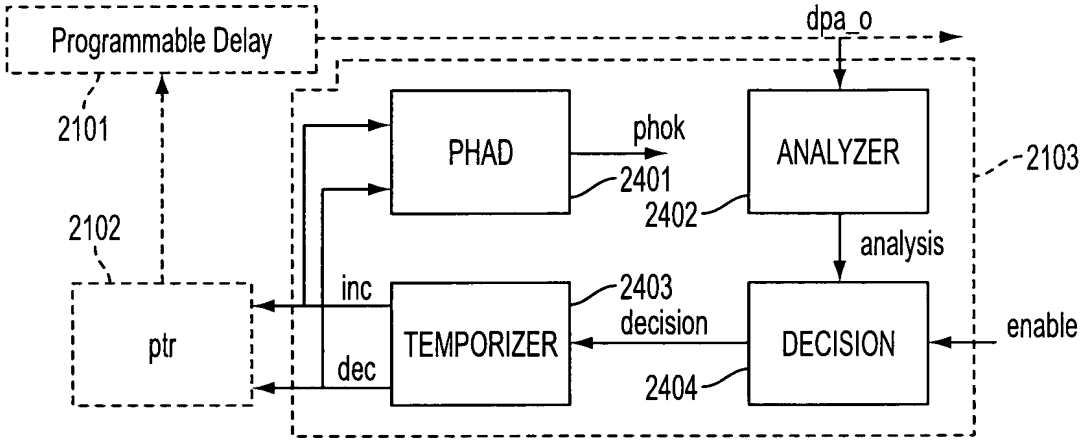

FIG. 24

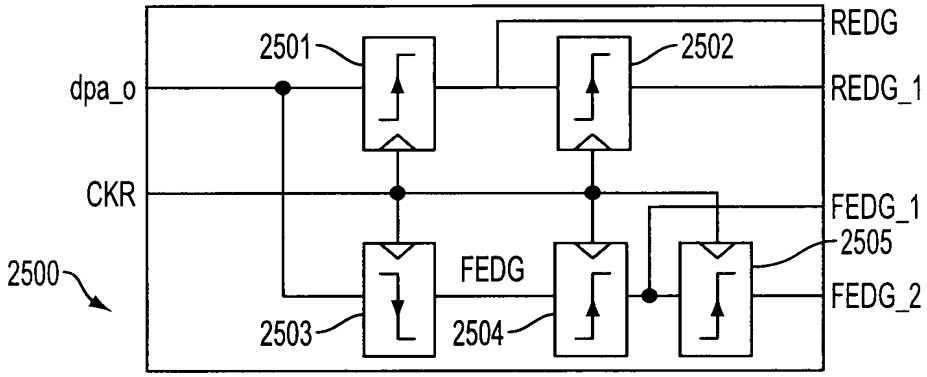

FIG. 25

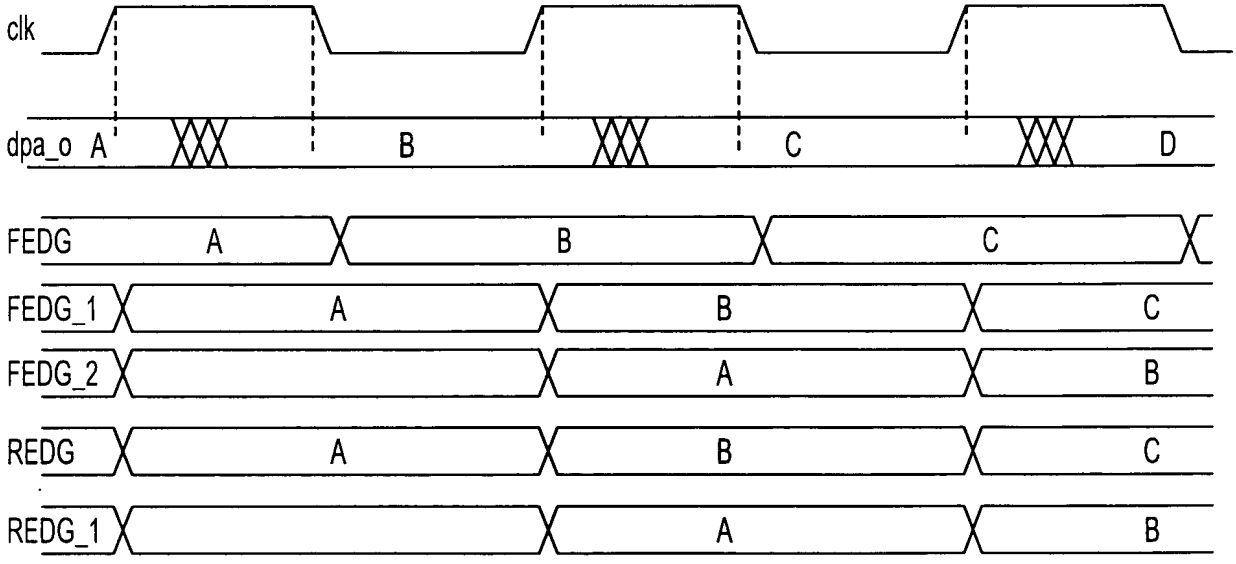

FIG. 26

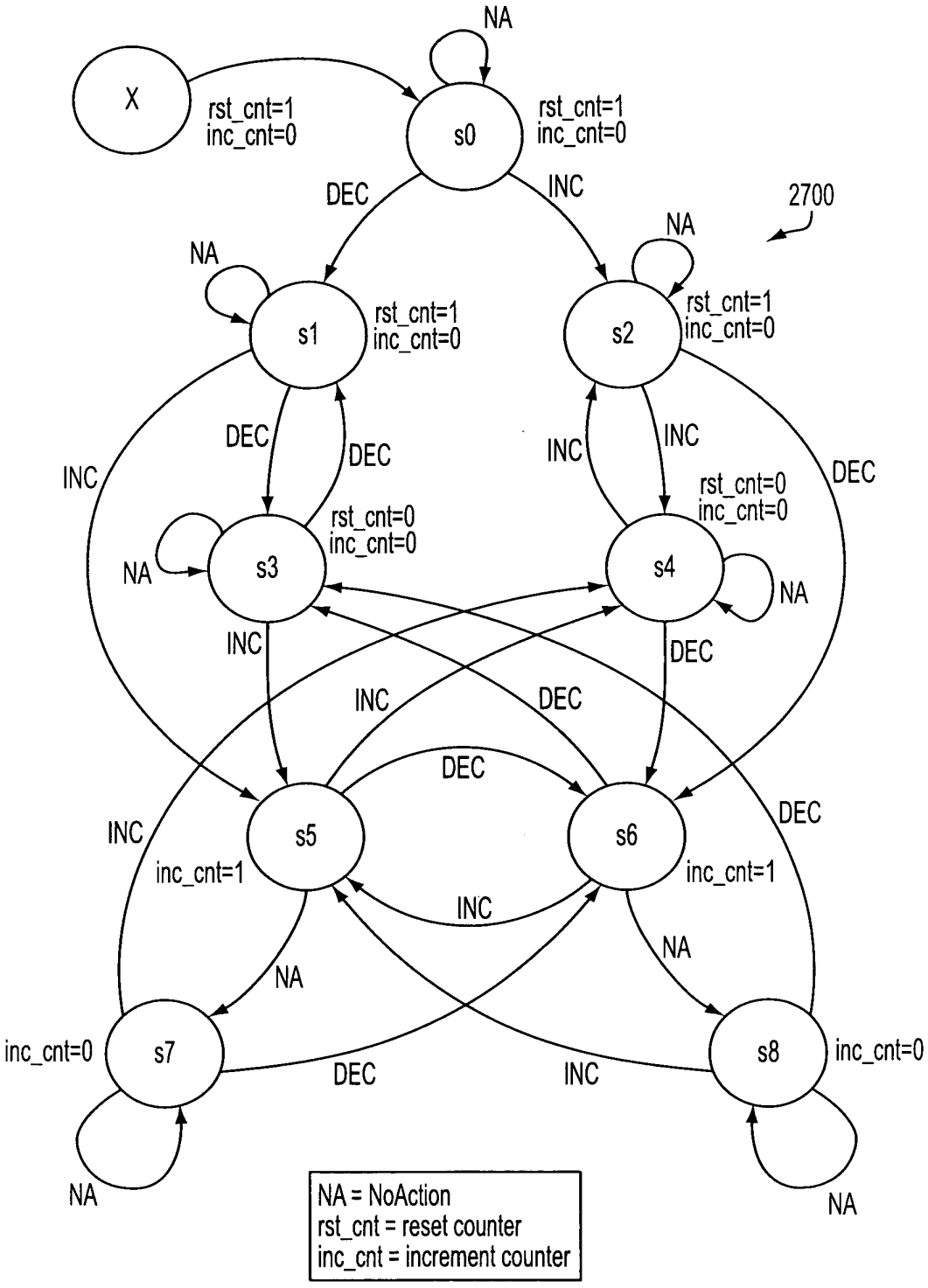
X
rst_cnt=1
inc_cnt=0
s0
rst_cnt=1
inc_cnt=0
NA
DEC
INC
2700
s1
rst_cnt=1
inc_cnt=0
s2
rst_cnt=1
inc_cnt=0
s3
rst_cnt=0
inc_cnt=0
s4
rst_cnt=0
inc_cnt=0
s5
inc_cnt=1
s6
inc_cnt=1
s7
inc_cnt=0
s8
inc_cnt=0
NA = NoAction
rst_cnt = reset counter
inc_cnt = increment counter

FIG. 27

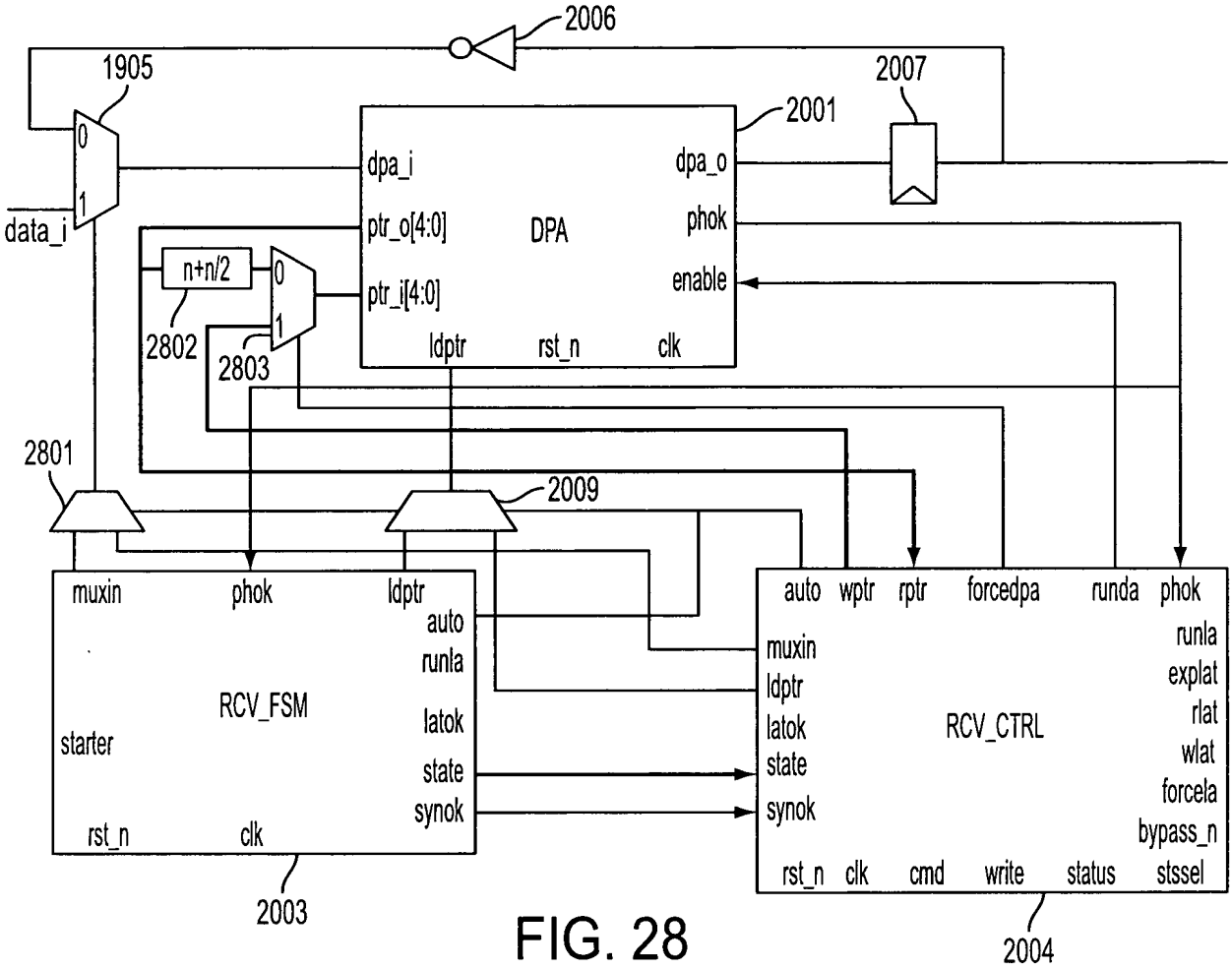
2006
1905
2007
2001
0
1
data_i
dpa_i
dpa_o
ptr_o[4:0]
DPA
phok
n+n/2
0
1
ptr_i[4:0]
enable
2802
2803
ldptr
rst_n
clk
2801
2009
muxin
phok
ldptr
auto
runla
RCV_FSM
latok
starter
state
synok
rst_n
clk
2003
auto
wptr
rptr
forcedpa
runda
phok
runla
muxin
explat
ldptr
rlat
latok
RCV_CTRL
wlat
state
forcela
synok
bypass_n
rst_n
clk
cmd
write
status
stssel
2004

FIG. 28

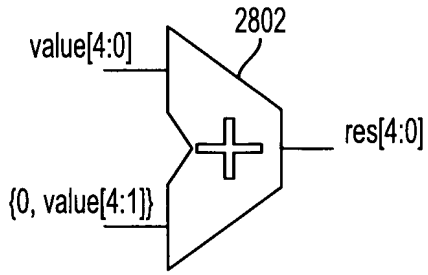
value[4:0]
2802
res[4:0]
{0, value[4:1]}

FIG. 29

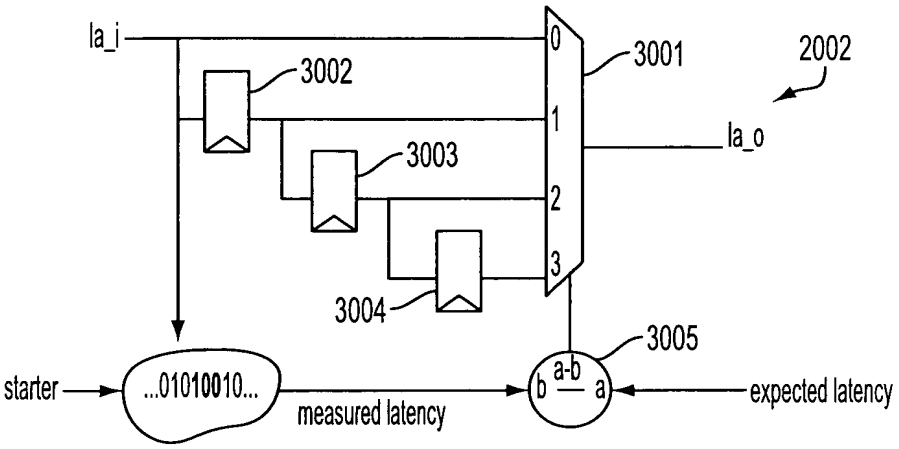
la_i
3002
3003
3004
0
1
2
3
3001
2002
la_o
3005
starter
...01010010...
measured latency
a-b
b
a
expected latency

FIG. 30

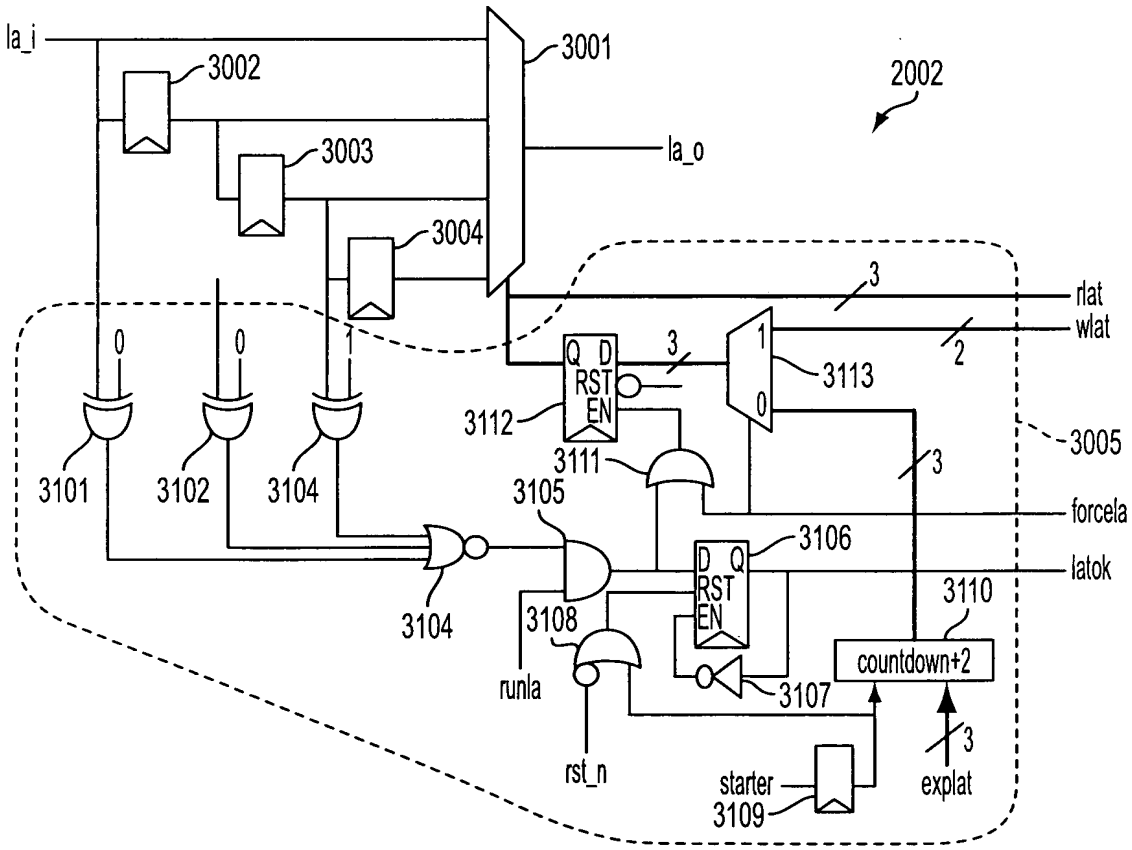
la_i
3002
3003
3004
3001
2002
la_o
3
rlat
wlat
2
0
0
1
3
Q D
RST
EN
3112
3111
1
0
3113
3005
3
3101
3102
3104
3105
forcela
3106
D Q
RST
EN
latok
3110
3104
3108
runla
3107
countdown+2
rst_n
starter
3109
3
explat

FIG. 31

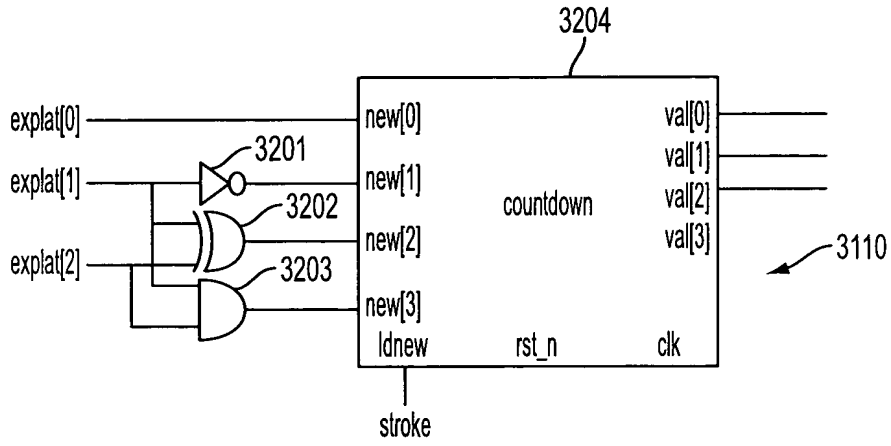
3204
explat[0]
explat[1]
explat[2]
3201
3202
3203
new[0]
new[1]
new[2]
new[3]
countdown
val[0]
val[1]
val[2]
val[3]
3110
ldnew
rst_n
clk
stroke

FIG. 32

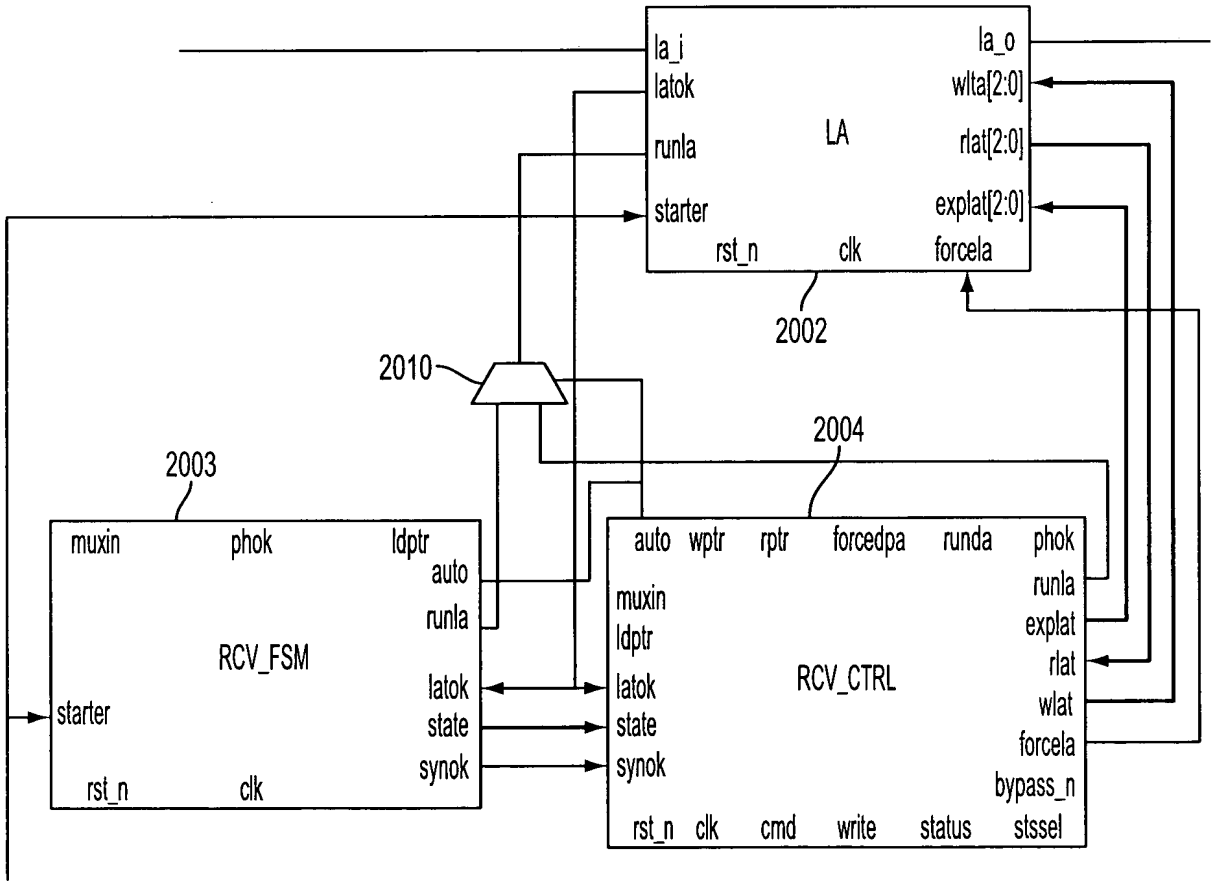
la_i
latok
runla
starter
rst_n
clk
LA
la_o
wlta[2:0]
rlat[2:0]
explat[2:0]
forcela
2002
2010
2003
2004
muxin
phok
ldptr
auto
runla
RCV_FSM
latok
state
synok
starter
rst_n
clk
auto
wptr
rptr
forcedpa
runda
phok
muxin
ldptr
latok
state
synok
RCV_CTRL
runla
explat
rlat
wlat
forcela
bypass_n
rst_n
clk
cmd
write
status
stssel

FIG. 33

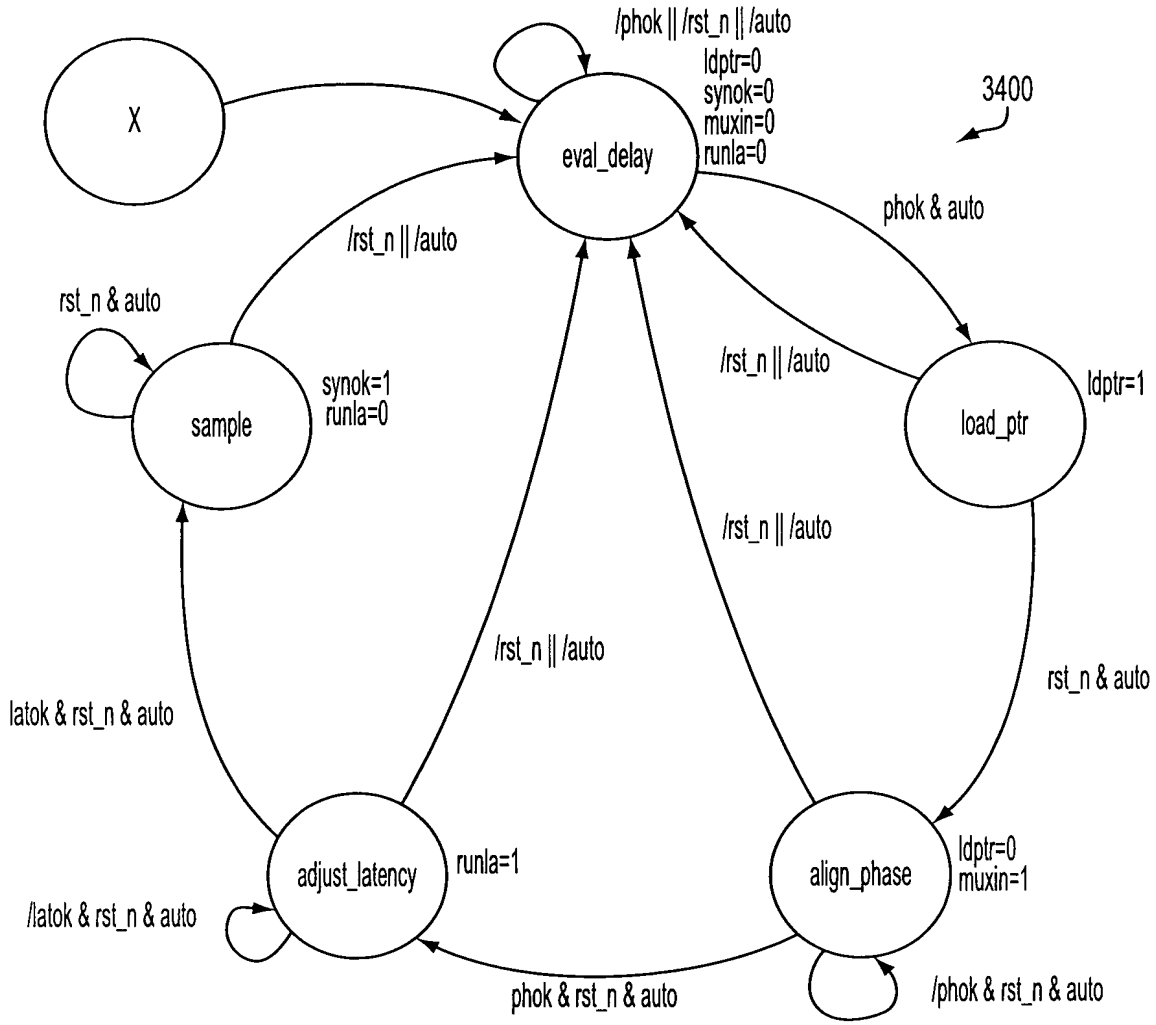

FIG. 34

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO

FIG. 35

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
XXXXXXXXXX		SYNOK	LATOK	PHOK	FSM_STATE			RLAT			RPTR				

FIG. 36

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

FIG. 37

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	X	0	EXPECTED LATENCY			X	0	X	X	X	X	X	X	X	1

FIG. 38

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	0	1	1	0	0	0	0	0	0	0

FIG. 39

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	0	0	0	0	0	0	0

FIG. 40

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	0	0	1	X	X	X	X	X	1	0

FIG. 41

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	X	X	X	X	X	0	0

FIG. 42

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	1	0	EXPECTED LATENCY			1	0	0	X	X	X	X	X	0	0

FIG. 43

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	X	X	X	X	X	0	0

FIG. 44

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	1	0	1	1	1	1	0	0	X	X	X	X	X	0	0

FIG. 45